AMENDMENTS TO THE SPECIFICATION:

Please substitute the following paragraph for paragraph 0002 on page 1.

--[0002] Increasingly miniaturized and high-density circuits necessitate that semiconductor device manufacturing projection exposure apparatuses be able to project circuit patterns on ~~rectiles~~ reticles onto wafer surfaces for exposure at even higher resolution. The projection resolution of a circuit pattern depends on the apertures (NA) of the projection optical system and on the exposing light wavelength, so methods are being employed for raising the resolution such as increasing the NA of the projection optical system or using light of a shorter wavelength for exposure. With regard to the later, the exposure light source has made transition from g rays to i rays, and from i rays to the excimer laser. Exposing devices using excimer laser with an oscillation wavelength of 248 nm and 193 nm are already in practical use.--

Please substitute the following paragraph for paragraph 0006 on pages 2 and 3.

--[0006] On the other hand, increased miniaturization of the circuit pattern means that highly-precise alignment between the ~~rectile~~ reticle upon which the circuit pattern is formed and the wafer upon which the pattern is cast is accordingly necessary. The required precision is 1/3 of the circuit line width, so with a current design using 180 nm for example, the required precision is 60 nm.--

Please substitute the following paragraph for paragraph 0007on page 3.

--[0007] Alignment in an exposure apparatus is performed by exposure transferring of alignment marks on the wafer at the same time as the circuit pattern on the ~~rectile~~ reticle, optically detecting the position of the alignment marks at the time of exposing the circuit pattern of the next rectile on the wafer, and positioning the wafer as to the rectile. Techniques for detecting the alignment includes a method wherein the alignment marks are enlarged and taken with a microscope so as to detect the position of the mark image, a method wherein diffraction grating is used as alignment marks so as to detect the phase of interference signals from interference with the diffraction light therefrom, thereby detecting the position of the diffraction grating, and so forth.--

Please substitute the following paragraph for paragraph 0014 on pages 6 and 7.

--[0014] Due to such an arrangement, even in the event that there are irregularities in the non-symmetry of alignment marks from one shot to another [[of]] or from one wafer to another at the time of executing global alignment, the measurement error due to the non-symmetry can be corrected based on measurement values measured under two different conditions, so measurement is not readily affected by structural change of the alignment marks due to the semiconductor processes, alignment precision can be improved, and yield in the semiconductor device manufacturing process can be improved. Further, the time for calculating the conditions for the semiconductor process which has been necessary in order to stabilize the shape of the alignment marks so far can be reduced, thereby improving the productivity of semiconductor device manufacturing, as well.--

Please substitute the following paragraph for paragraph 0040 on page 10.

--[0040] Fig. 1 is a schematic diagram of a semiconductor exposure apparatus according to the present invention. Note that only the portions necessary for describing the embodiments are shown, and the other portions are omitted in the drawings. The exposure apparatus 1 is configured of a reduction projection optical system 11 for reduced projection of a ~~rectile~~ reticle 10 upon which a circuit pattern has been drawn, a wafer chuck 13 for holding a wafer 12 upon which a base pattern and alignment marks have been formed in a previous processes, a wafer stage 14 for positioning the wafer 12 to a predetermined position, an alignment detection optical system 15 for measuring the position of the alignment marks on the wafer, and so forth.--

Please substitute the following paragraph for paragraph 0044 on pages 13 and 14.

--[0044] Now, the alignment mark image taken in this way is processed with alignment signal processing means 16 as described below. Template matching is used for calculating the alignment mark position used with the present embodiment. With template matching, correlation computation is performed between the obtained signals which are indicated by S in Fig. 6B and the template T shown in Fig. 6A which the apparatus has beforehand, wherein the position with the highest correlation is detected as the center of the positioning mark. In the correlation value function indicated by E in Fig. 6C, resolution of 1/10 to 1/50 pixels can be achieved by obtaining the center-of-gravity pixel position of an area of several pixels in the horizontal direction from the peak pixel. Template matching is expressed by the following Expression.

[Expression 1]

$$E(X) = \frac{1}{\sum_{J=-k}^{k} [\, S(X+J) - T(J)\,]^2}$$

wherein S represents ~~singles~~ signals obtained with the sensor, T represents the template, and E represents the correlation results.--

Please substitute the following paragraph for paragraph 0060 on pages 20, 21 and 22.

--[0060] Next, the method for obtaining this non-symmetry error correction coefficient a will be described. A first method is to measure each sample shot under the first measurement conditions and second measurement conditions at the time of the above-described AGA (global alignment),

store the measurement values and residual Ri for each shot, substitute the measured values (xi, yi) measured under the first measurement conditions at each sample shot and the alignment mark design positions (Xi, Yi) in the Expressions 8 and 9 to obtain the AGA parameters (Sx, Sy, qx, qy, Bx, By), and position each of the shots on the wafer 12 based on the AGA parameters, following which exposing is performed. At this time, a first overlaying evaluation mark is formed on the wafer 12 along with the alignment mark 50, and a second overlaying evaluation mark on the ~~rectile~~ reticle 10 is transferred by exposure onto the resist on the first overlaying evaluation mark following AGA alignment. The positional offset amount of the first and second overlaying evaluation marks is measured for a sample shot for the AGA using a overlaying precision evaluation device. Fig. 11 shows the relation of these measurement values. The correction residual Ri (wherein i is the shot No.) measured by AGA and the measurement value Ki (wherein i is the shot No.) measured by the overlaying precision evaluation device should match with opposite signs, but in the event that there is non-symmetry in the alignment mark, these do not match by a error component ei due to the non-symmetry. The error component ei can be obtained by ei = Ri + Ki (wherein i is the shot No.). Next, the relation between the error component ei, and the difference value dMi (i.e., M1i - M2i) of the measurement value M1i under the first measurement conditions and the measurement value M2i under the second measurement conditions, is obtained. Fig. 12 illustrates the correlation of the values of dMi and ei for each shot and an approximation line obtained by the least-square method. Thus, an approximation line is obtained by the least-square method from the difference value (M1i - M2i) and the error component (Ri + Ki), and the inclination thereof is denoted by α. This method determines the

value of the correction coefficient a based on the overlaying precision evaluation device. Also, those skilled in the art will be able to readily apply methods other than using an overlaying precision evaluation device, such as a method for obtaining the offset amount Ki following exposure based on electrical properties called electric measurement, a method for obtaining Ki using a measuring SEM, and so forth.--

Please substitute the following paragraph for paragraph 0065 on page 24.

--[0065] The wafer is positioned as to the exposure system based on the AGA measurement values calculated in Step 59, and the pattern on the ~~rectile~~ reticle is transferred by exposure onto the wafer in Step 60.--